

REMARKS/ARGUMENTS

Favorable consideration of this application, in light of the following discussion, is respectfully requested.

Claims 11-17 are pending in the application.

In the Office Action, Claims 11, 12, 15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley et al. (DE 3142591, hereinafter "Turley") in view of Tsuzuki et al. (EP 0263711, hereinafter "Tsuzuki"); Claims 13 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley and Tsuzuki in view of Kobayashi (Patent No. 5,736,779); and Claims 11-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Quigley et al. (U.S. Patent No. 5,708,288, hereinafter "Quigley") in view of Pequignot et al. (U.S. Patent No. 6,157,530, hereinafter "Pequignot").

Applicants request acknowledgement of the Information Disclosure Statement (IDS) filed on October 25, 2001.

Briefly recapitulating, Claim 11 is directed to a device for protection of an electronic component against electrostatic discharges. The device includes a plurality of Zener diodes formed in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer and having two regions of heavy doped opposite conductivity types with at least one of the two regions extending to the insulating layer. The device also includes a contact pin connected to the electronic component and connected through the Zener diodes to ground in order to divert an electrostatic discharge and thereby protect the electronic component. The plurality of Zener diodes are connected in series and are disposed so as to be directly polarized. By embedding a plurality of Zener diodes in a substrate, a sufficient number Zeners may be compactly arranged in series to resist power supply voltages without any inducing excessive leakage.¹ The advantages of Applicants' invention are to provide

¹ Specification, page 14, lines 1-5 and lines 14-18; Figures 4-6.

protection with very good efficiency.² This protection is provided with a device having very low resistance.³

By way of background, as defined in Applicant's specification in claims, the term "directly polarized" means that a) all the Zener diodes are polarized in the same forward direction and b) in normal use of the circuit, the p-region of a junction is at a potential greater than the n-region of a junction.⁴

Turley describes an over voltage protection circuit that includes a series of oppositely charged p/n junctions.⁵ In particular, Turley describes a circuit that includes a plurality of serially connective Zener diodes arranged in opposing plurality (e.g., diodes 55-59 shown in Figure 5). However, Turley does not disclose or suggest Applicants' claimed feature of plural Zener diodes connected in series and disposed so as to be directly polarized. These n⁺/p diodes are realized in the same silicon substrate and are in turn biased backwards and forward. That is, these n⁺/p diodes are in opposing polarity and are not directly polarized as recited in Applicants' claims.

Furthermore, Turley does not disclose heavily built regions on each side of a junction as required so that, in normal use of the circuit, the p-region of a junction is at a potential greater than the n-region of a junction. Figure 7 of Turley shows a p doped zone but does not disclose or suggest p⁺ doped zone. Thus, in Turley, the gate of a MOS transistor is protected by n⁺/p diodes mounted in series.⁶ Thus, for another reason, Turley does not disclose or suggest Applicants' claimed 'directly polarized' diodes.

² Specification, page 16, line 28 to page 17, line 15.

³ Specification, page 11, Table 1.

⁴ Specification, page 15, line 30 – page 16, line 16.

⁵ Turley, abstract.

⁶ Turley, Figure 5.

Tsuzuki describes a circuit where the Zener diodes are mounted in series and are biased in the same direction.⁷ However, contrary to the assertion in the Office Action, these diodes are backward biased and not forward biased.⁸ It is common to bias Zener diodes since the peculiarity of Zener diodes is to have an adjustable backward breakdown voltage. The aim of Tsuzuki is to optimize a circuit by passing from an annular structure (where the diodes correspond to concentric rings) to a parallel structure.⁹ This allows the avoidance of corner portions of the junctions which constitute weak points in the protection.¹⁰ However, because the diodes of Tsuzuki are backward biased and not forward biased, the diodes are not 'directly polarized' as recited in Applicants' claims.

The Official Action asserts that because opposite direction diodes of Tsuzuki are shorted, the resultant chain is a series of directly polarized Zener diodes. Applicants note that Tsuzuki expressly describe the diodes as oppositely polarized. Thus, Applicants' traverse the characterization in the Official Action and assert that this finding is based on an impermissible hindsight reconstruction of Applicants' invention. Applicants also consider the characterization in the Official Action to be an assertion of inherency. However, Applicant respectfully submits that the assertion of inherency is insufficient to show that Tsuzuki inherently teaches Applicants' claimed directly polarized Zener diodes because the rejection fails to show "that the alleged inherent characteristic necessarily flows from the teachings of the applied prior art"¹¹ "The fact that a certain result may occur or be present in

⁷ Tsuzuki, Figure 6.

⁸ Tsuzuki, column 7, lines 6-7; Figures 10, 12, 10A, 10B; column 2, lines 28-31.

⁹ Tsuzuki, Figure 3.

¹⁰ Tsuzuki, column 6, lines 57-61.

¹¹ See MPEP 2112 (emphasis in original) (citation omitted). See also same section stating that "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic," (emphasis in original). See also In re Robertson, 49 USPQ2d 1949, 1951 (Fed. Cir. 1999) ("[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill,'" citing Continental Can Co. v. Monsanto Co., 948 F2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991); and "[i]nherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient," Id. at 1269 (citation omitted)).

the prior art is not sufficient to establish inherency of that result or characteristic.”¹² “To establish inherency, the extrinsic evidence ‘must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.’”¹³

MPEP §706.02(j) notes that to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Also, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Without addressing the first two prongs of the test of obviousness, Applicants submit that the Official Action does not present a *prima facie* case of obviousness because both Turley and Tsuzuki fail to disclose all the features of Applicants’ claimed invention.

Applicants have also considered Kobayashi and submit Kobayashi does not cure the deficiencies of Turley and Tsuzuki. Kobayashi describes a semiconductor device with double Zener diode 19 disposed between a gate and a source of a MOS type semiconductor device, where the double Zener diode has the following arrangement: $n^+/p/p^+/p/n^+$. With this arrangement double Zener diode 19 is characterized as having opposing polarity, not direct polarity as recited in Applicants’ claims. Thus like Turley, Kobayashi does not disclose or

¹² *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1995, 1957 (Fed. Cir. 1993).

¹³ *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

suggest Applicants' claimed feature of a plurality of Zener diodes mixed in series and disposed so as to be directly polarized.

Quigley describes a thin film silicone on insulator circuit for Zener diodes 26, 27, 28 and 29 in a low voltage triggering apparatus (LVTA) 36, where the LVTA 36 is a Zener diode formed within the boundaries of a surface silicone control rectifier 30 and includes p⁺ doped Zener region 242, field oxide regions 145, and ⁻ doped Zener region 244, and ⁺ doped region 244.¹⁴ LVTA 36 is a single Zener diode formed in the boundaries of surface silicone control rectifier 30. As acknowledged in the Office Action, Turley does not disclose Applicants' claim plurality of Zener diodes. The Zener diodes of Quigley are also polarized in inverse. Pequignot describes a circuit wherein a diode string is mounted between two power rails V_{DD1} and V_{DD2}. However, contrary to the Office Action, Pequignot does not use Zener diodes.

Thus, like the combination of Turley and Tsuzuki, the combination of Quigley and Pequignot does not disclose or suggest the invention recited in Applicants' Claim 11. As none of the cited prior art, individually or in combination, disclose or suggest all the elements of independent Claim 11, Applicants submit the inventions defined by Claim 11, and all claims depending therefrom, are not rendered obvious by the asserted references for at least the reasons stated above.¹⁵

Furthermore, Applicants submit there is no teaching, suggestion, or motivation, either explicitly or implicitly, in either reference to combine the teachings of Turley and Tsuzuki or the teachings of Quigley and Pequignot to arrive at Applicants' inventions recited in Claim

¹⁴ Quigley, column 3, lines 2-11; column 4, lines 9-22; Figures 1-3.

¹⁵ MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

11. Thus, Applicants submit it is only through an impermissible hindsight reconstruction of Applicants' invention that the rejection of Claim 11 can be understood.¹⁶

Finally, assuming *arguendo* there is motivation to combine the teachings of Turley and Tsuzuki or the teachings of Quigley and Pequignot, there is no reasonable expectation that the resulting circuit would be functional. That is, there is no reasonable expectation that replacing the oppositely charged p/n junctions of Turley with the backward biased junctions of Tsuzuki would result in functional circuit. Similarly, there is no reasonable expectation that replacing the single Zener diode of Quigley with the diode string of Pequignot would result in functional circuit.

Accordingly, in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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¹⁶ MPEP § 2143.01 "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge of one of ordinary skill in the art."